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81 System-level power optimization: techniques and tools

Luca Benini, Giovanni de Micheli

April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2

Full text available: pdf(385.22 KB) Additional Information: full citation, abstract, references, citings, index terms

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

82 Using VRML in construction industry applications

Robert Lipman, Kent Reed

February 2000 **Proceedings of the fifth symposium on Virtual reality modeling language (Web3D-VRML)**

Full text available: pdf(945.65 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes initial research using the Virtual Reality Modeling Language (VRML97) in construction industry applications. The modeling of steel structures and construction equipment as objects for inclusion in construction-site world models was studied. The ultimate goal is to provide three-dimensional web-based technologies for managing, accessing, and viewing construction project information.

Keywords: VRML, computer-integrated construction, construction equipment, steel structures, virtual environments

83 300MHz design methodology of VU for emotion synthesis

Takayuki Kamei, Hideaki Takeda, Yukio Ootaguro, Takayoshi Shimazawa, Kazuhiko Tachibana, Shin'ichi Kawakami, Seiji Norimatsu, Fujio Ishihara, Toshinori Sato, Hiroaki Murakami, Nobuhiro Ide, Yukio Endo, Akira Aono, Atsushi Kunimatsu

January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**

Full text available: pdf(509.23 KB) Additional Information: full citation, references, citings

84 Memory binding for performance optimization of control-flow intensive behaviors

Kamal S. Khouri, Ganesh Lakshminarayana, Niraj K. Jha

November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(164.71 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a memory binding algorithm for behaviors that are characterized by the presence of conditionals and deeply-nested loops that access memory extensively through arrays. Unlike previous works, this algorithm examines the effects of branch probabilities and allocation constraints. First, we demonstrate, through examples, the importance of incorporating branch probabilities and allocation constraint information when searching for a performance-efficient memory binding. We als ...

85 Synthesis of asynchronous control circuits with automatically generated relative timing assumptions

Jordi Cortadella, Michael Kishinevsky, Steven M. Burns, Ken Stevens

November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(242.64 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a method of synthesis of asynchronous circuits with relative timing. Asynchronous communication between gates and modules typically utilizes handshakes to ensure functionality. Relative timing assumptions in the form "event a occurs before event b" can be used to remove redundant handshakes and associated logic. This paper presents a method for automatic generation of relative timing assumptions from the unt ...

86 Modeling design constraints and biasing in simulation using BDDs

Jun Yuan, Kurt Shultz, Carl Pixley, Hillel Miller, Adnan Aziz

November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(133.50 KB) Additional Information: full citation, abstract, references, citings, index terms

Constraining and input biasing are frequently used techniques in functional verification methodologies based on randomized simulation generation. Constraints confine the simulation to a legal input space, while input biasing, which can be considered as a probabilistic constraint, makes it easier to cover interesting "corner" cases. In this paper, we propose to use constraints and biasing to form a simulation environment instead of using an expli ...

87 Sketching with projective 2D strokes

Osama Tolba, Julie Dorsey, Leonard McMillan

November 1999 **Proceedings of the 12th annual ACM symposium on User interface software and technology**

Full text available: pdf(545.06 KB) Additional Information: full citation, abstract, references, citings, index terms

Freehand sketching has long had appeal as an artistic medium for conceptual design because of its immediacy in capturing and communicating design intent and visual experience. We present a sketching paradigm that supports the early stages of design by preserving the fluidity of traditional freehand drawings. In addition, it attempts to fill the gap between 2D drawing programs, which have fixed views, and 3D modeling programs that allow arbitrary views. We implement our application as a two- ...

Keywords: grids, illustration, panoramas, perspective, vanishing points, view alignment

88 Human-guided simple search: combining information visualization and heuristic search

David Anderson, Emily Anderson, Neal Lesh, Joe Marks, Ken Perlin, David Ratajczak, Kathy Ryall

November 1999 **Proceedings of the 1999 workshop on new paradigms in information visualization and manipulation in conjunction with the eighth ACM internation conference on Information and knowledge management**

Full text available: pdf(937.14 KB) Additional Information: full citation, abstract, references, index terms

Scheduling, routing, and layout tasks are examples of hard operations-research problems that have broad application in industry. Typical algorithms for these problems combine some form of gradient descent to find local minima with some strategy for escaping nonoptimal local minima and traversing the search space. Our idea is to divide these two subtasks cleanly between human and computer: in our paradigm of human-guided sample search the computer is responsible only for fin ...

Keywords: combinatorial optimization, computer-human interaction, informtaion visualization, interactions systems, operations research, vehicle routing

89 Equivalent Elmore delay for RLC trees

Yehea I. Ismail, Eby G. Friedman, Jose L. Neves

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available: pdf(110.99 KB) Additional Information: full citation, references, citings, index terms

90 Enhancing simulation with BDDs and ATPG

Malay K. Ganai, Adnan Aziz, Andreas Kuehlmann

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available: pdf(795.60 KB) Additional Information: full citation, references, citings, index terms

Keywords: ATPG, BDDs, coverage, formal verification, simulation

91 Gradient-based optimization of custom circuits using a static-timing formulation

A. R. Conn, I. M. Elfadel, W. W. Molzen, P. R. O'Brien, P. N. Strenski, C. Visweswariah, C. B. Whan

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

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92 ipChinook: an integrated IP-based design framework for distributed embedded systems

Pai Chou, Ross Ortega, Ken Hines, Kurt Patridge, Gaetano Borriello

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

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93 Formal verification in hardware design: a survey

Christoph Kern, Mark R. Greenstreet

April 1999 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 4 Issue 2

Full text available: pdf(411.53 KB) Additional Information: full citation, abstract, references, citings, index terms

In recent years, formal methods have emerged as an alternative approach to ensuring the quality and correctness of hardware designs, overcoming some of the limitations of traditional validation techniques such as simulation and testing. There are two main aspects to the application of formal methods in a design process: the formal framework used to specify desired properties of a design and the verification techniques and tools used to reason about the relationship between a spec ...

Keywords: case studies, formal methods, formal verification, hardware verification, language containment, model checking, survey, theorem proving

94 Procedure cloning: a transformation for improved system-level functional partitioning

Frank Vahid

January 1999 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 4 Issue 1

Full text available: pdf(227.98 KB) Additional Information: full citation, abstract, references, citings, index terms

Functional partitioning assigns the functions of a system's program-like specification among system components, such as standard-software and custom-hardware processors. We introduce a new transformation, called procedure cloning, that significantly improves functional partitioning results. The transformation creates a clone of a procedure for sole use by a particular procedure caller, so the clone can be assigned to the caller's processor, which in turn improves performance through reduced ...

Keywords: behavioral synthesis, embedded systems, functional partitioning, hardware/software codesign, replication, system-level design, system-on-a-chip, transformations

95 Transforming control-flow intensive designs to facilitate power management

Ganesh Lakshminarayana, Anand Raghunathan, Niraj K. Jha, Sujit Dey

November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(1.09 MB) Additional Information: full citation, references, index terms

96 Integrating logic retiming and register placement

Tzu-Chieh Tien, Hsiao-Pin Su, Yu-Wen Tsay, Yih-Chih Chou, Youn-Long Lin

November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(440.79 KB) Additional Information: full citation, references, citings, index terms

97 A graph-partitioning-based approach for multi-layer constrained via minimization

Yih-Chih Chou, Youn-Long Lin

November 1998 **Proceedings of the 1998 IEEE/ACM international conference on**

Computer-aided design

Full text available: pdf(414.86 KB) Additional Information: full citation, references, citings, index terms

98 Fast high-level power estimation for control-flow intensive design

Kamal S. Khouri, Ganesh Lakshminarayana, Niraj K. Jha

August 1998 **Proceedings of the 1998 international symposium on Low power electronics and design**

Full text available: pdf(901.04 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present a power estimation technique for control-flow intensive designs that is tailored towards driving iterative high-level synthesis systems, where hundreds of architectural trade-offs are explored and compared. Our method is fast and relatively accurate. The algorithm utilizes the behavioral information to extract branch probabilities, and uses these in conjunction with switching activity and circuit capacitance information, to estimate the power consumption of a given ...

99 FACT: a framework for the application of throughput and power optimizing transformations to control-flow intensive behavioral descriptions

Ganesh Lakshminarayana, Niraj K. Jha

May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

Full text available: pdf(341.78 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present an algorithm for the application of a general class of transformations to control-flow intensive behavioral descriptions. Our algorithm is based on the observation that incorporation of scheduling information can help guide the selection and application of candidate transformations, and significantly enhance the quality of the synthesized solution. The efficacy of the selected throughput and power optimizing transformations is enhanced by the ability of our algorit ...

Keywords: high-level synthesis, telecommunication

100 Synthesis of power-optimized and area-optimized circuits from hierarchical behavioral descriptions

Ganesh Lakshminarayana, Niraj K. Jha

May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

Full text available: pdf(310.50 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

We present a technique for synthesizing power- as well as area-optimized circuits from hierarchical data flow graphs under throughput constraints. We allow for the use of complex RTL modules, such as FFTs and filters, as building blocks for the RTL circuit, in addition to simple RTL modules such as adders and multipliers. Unlike past techniques in the area, we also customize the complex RTL modules to match the environment in which they find themselves. We present a fast and efficient algor ...

Keywords: ISM frequency band, RF CMOS, digital radio, spread spectrum communication, transceiver

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